Fundamentals of Instantaneous-Values-Based Busbar Differential Protection

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***Abstract*—This paper aims to present a general overview of principles of low impedance busbar protection against typical faults in busbars with dynamic configuration. Based on instantaneous values, traditional 1-out-of-1 and 2-out-of-2 tripping logics are detailed. This technique performed a well response for internal faults, it was able to discriminate external faults, to recognize the current transformer (CT) saturation, as well as to detect evolving faults. Additionally, a small power system was conveniently adopted to show step by step the formation of a suitable zone selection logic. Besides, it is also explained in a general way how the success of this strategy depends directly on the switches status. For the purposes of this work, several faults were applied to a power system, modeled in Alternative Transient Program (ATP). The results show the applicability of the implemented logics to overcome typical faults in busbars and to recognize normal technical procedure.**

***Keywords*—CT saturation, busbar, differential protection, zone selection**

I. Introduction

Due to increasing demand, electrical stations should be adequate for connection of more subsystems. It meant the development of more sophisticated relaying schemes, discriminative, selective and capable to actuate rapidly, in order to assure the service's continuity and the system's stability.

Bus differential protection schemes can be principally constituted by high impedance or numerical low impedance relays. However, microprocessor-based relaying provides the ability to clear the fault rapidly and to dynamically reconfigure the protection zone [1], [2]. According to the measurement technique, numerical busbars protection based in instantaneous sampled values is more adequate than phasor estimation due its faster response [3]. Nevertheless, both elements can be used complementarily to add security to the algorithm [4].

Howsoever, independently of the technique, the design of a relaying scheme must consider several scenarios. In-zone faults, external faults and evolving faults are the most studied cases [5]. Nevertheless, one important challenge for bus protection is the CT saturation, caused by the merging of the decaying DC component and current contributions from bays connected to the bus [6], [7] . Additionally, other factors as fault type, fault resistance, inception angle and the effect of feeders must be also considered [8], [9].

By adopting more complex busbars arrangements, a dynamic zone selection function should be integrated in relays to avoid unnecessary disconnections [10]. It means that an advanced zone selection must be capable of assign inputs currents to the appropriate differential element and determines the breakers to trip in the event of a busbar fault [11].

The tripping logic supported by a dynamic zone selection must also consider practical items. The location, polarity and ratios of CTs, the creation of *blind spots* and *stub bus* zones are common issues [12]. Besides, the busbars parallelism condition in a circuit transfer procedure, and the protection transfer when a breaker is substituted, are some well-known concerns mentioned in [13].

In this context, this work tries to give to readers the basic knowledges of the low impedance differential bus protection. Aiming to do so, a dynamic zone selection logic is firstly introduced to overcome the complexity of busbars arrangements. Also, a brief introduction of how to determine the disconnect switch status is presented. The described protection algorithm uses the tripping logics 1-out-of-1 and 2-out-of-2, based on instantaneous values of currents. Typical faults in busbars were simulated by using a power system modeled in ATP. The results show the effectiveness of the algorithm for internal, external and evolving faults considering the CT saturation.

II. Fundamentals of busbar differential protection

Numerical low-impedance busbar differential relays are based on the Kirchhoff's current law. In a general way, the differential element compares an operating current, i_{op}, with a restraining current, i_{res}, in order to distinguish between internal and external faults to the protection zone. In that sense, the correct assignment of the currents for calculations, as well as the recognition of disconnect switches status, are critical tasks.

A. Zone selection logic

For any busbars arrangement, the bus protection zones are defined by the location of CTs. However, the bus zone opened during fault elimination is defined by the breakers surrounding the bus. Therefore, the protection zones will be defined by the CTs surrounding the current paths, which are defined by switches status. Aiming to show the procedure to establish a zone selection logic, the power system with a double bus single breaker arragenment illustrated in Fig. 1 is used.

The busbar configuration is a double-bus single breaker. In this example both busbars, A and B, are energized, i.e. any

TABLE I
ASSIGNMENT OF LOGIC STATES OF FLAGS

Branch	CT	f_k^A	f_k^B	f_k^{AB}
L1	CT1	(S1L1 AND (CB1 OR SB1)) OR ((BP) AND (CB1 OR SB1))	(S2L1 AND (CB1 OR SB1)) OR ((BP) AND (CB1 OR SB1))	CB1 OR (SB1 AND CCB)
L2	CT2	(S1L2 AND (CB2 OR SB2)) OR ((BP) AND (CB2 OR SB2))	(S2L2 AND (CB2 OR SB2)) OR ((BP) AND (CB2 OR SB2))	CB2 OR (SB2 AND CCB)
Coupling	CTC1	Never	$\overline{BP}$ AND CCB	Never
	CTC2	$\overline{BP}$ AND CCB	Never	Never

network element can be connected to either busbar. The first key task is to determine the selector switches to be closed for connection of network elements to a certain bus. In this case, the bay L1 is normally connected to bus A through S1L1 closed. Analogously, the circuit L2 is connected to bus B by closing S2L2. To complete the branches connection, each bay is directly connected to the busbars by using their respective circuit breakers, CB1 and CB2.

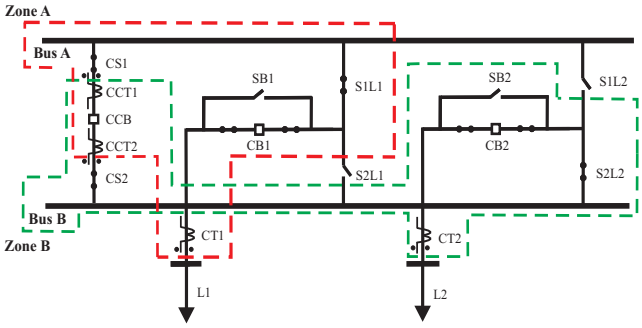

Fig. 1. Bus arrangement for selection zone logic example

On the other hand, if any circuit breaker is isolated for a substitution or maintenance procedure, the bypass disconnect switches, SB1 and SB2, are used to maintain the current flow. In this situation, the tie breaker, CCB, is used to guarantee that the new current path will be part of a zone protection. In this coupler branch, the polarities of CTs, CCT1 and CCT2, were adopted in such a way that creates a superimposed zones, eliminating blind spots near the bus coupler. As a consequence, the individual protection zones of buses A and B will be seen by CCT2 and CCT1, respectively. In turn, supposing the breaker CB2 needs to be replaced, the fault clearance will be performed by CCB and the measurement of currents will be done by CCT1.

In this example, busbars are normally interconnected by maintaining the breaker and switches of bus coupler normally closed. In other scenario, one busbar can be energized, while the other one is defined as a transfer bus. Either case includes closing their respective selector switches simultaneously, in order to avoid the service interruption during a circuit transfer. In this situation, spurious currents may flow in busbars without being measured. This parallelism condition, BP, can lead to a false trip and, consequently, must be included on the selection zone logic. In order to do so, it must be verified that, at least, two selector switches of one branch are closed, as well as the bus coupler is also closed.

BP = [(S1L1 AND S2L1) OR (S1L2 AND S2L2))] AND [(CS1 AND CS2) AND (CCB)].

Additionally, protection scheme must be able to overcome the breakers failure. For that, a check zone, Z_{AB}, is used to supervise the overall current balance of the busbars structure composed by multiple protection zones. This additional stage of zone selection logic is independent of selective switches and do not use auxiliary contacts [12].

For the assignment of the bus coupler status, it must be noted that CCT1 will never measure the currents in bus A, as well as CCT2 is out of the protection zone of the bus B. That also means that the check zone can not be performed by coupler branch elements. Nevertheless, for the attribution of flags of these CTs currents to a differential element, it must be verified that the coupler circuit breaker is closed and there is not parallelism between busbars. Therefore, the complete logic to set the currents flags status are shown in Table I.

The assignment of the correct differential element of the phase F of bay k, located in the zone Z, will be represented by adopting the *enabling flags*, f_k^Z, as shown in Table I. By using this flags, it is possible to compute the operation current, $i_{op}^{Z_F}$ and the restraint current $i_{res}^{Z_F}$ for each protection zone as follows

$$i_{op}^{Z_F} = \left| \sum_{k=1}^{n} f_k^Z \cdot i_k^F \right| , \tag{1}$$

$$i_{res}^{Z_F} = \sum_{k=1}^{n} f_k^Z \cdot \left| i_k^F \right| , \tag{2}$$

In order to issue a trip command for the correct circuit breakers, the zone where the fault is detected and the selector switches status must be verified. Complementary, the check zone might also detect the fault. Table II shows the tripping logic of each circuit breaker of the evaluated power system, in which Z_A, Z_B and Z_{AB} represents the trip status of the protection zones.

With a bay in-service, the actual signals of current and switches position are transmitted to central unit. In the case of bay out-of-service, the switches position perceived by relay is open and the value of current sent for zone selection logic is zero, but the actual value is taken by the check zone logic, as a safety measure in the event of the operational failure of the circuit breaker.

TABLE II
CIRCUIT BREAKERS OPERATION LOGIC

CB	Logic
CB1	[(Z_A AND S1L1) OR (Z_B AND S2L1)] AND Z_{AB}
CB2	[(Z_A AND S1L2) OR (Z_B AND S2L2)] AND Z_{AB}
CCB	(Z_A OR Z_B) AND Z_{AB}

B. Disconnect Switches Status

The flags of currents of a reconfigurable bus arrangement depends on the status of disconnect switches. That means that the correct assignment to, or remotion from, CTs for calculations will depend on the switch status signal entering in relay.

The determination of switches status is performed by using two auxiliary contacts, whose complete logic is presented in Table III. As shown in Fig. 2, an open switch means that contact 89A is open and contact 89B is closed. In this conditions, CT current is not taken into account by relay. Analogously, if 89A is closed and 89B is open, switch is in closed status. In this case, the CTs currents are assign to relay for calculations in differential element [12].

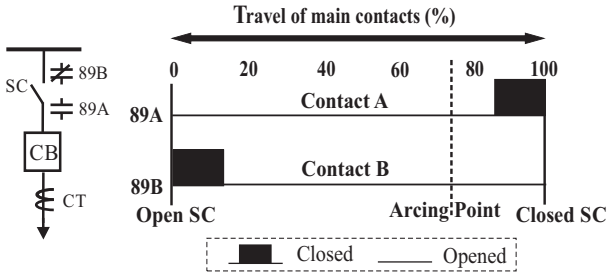

Fig. 2. State of auxiliary contacts of disconnect switches

In practice, the electric arc is a phenomenon inherent to switching. As a consequence, this current starts to flow in disconnect travel path before fully completing an open-to-close procedure. Likewise, current can be maintained during some time after starting a close-to-open operation.

Once the arc current is not measured by protection scheme, it is important to determine the flags of currents without considering it. Thus, relay must assigns the currents before attaining the arcing point in an open-to-close operation, or remove them after passing the arcing point in a open-to-close procedure.

TABLE III
INTERPRETATION OF DISCONNECT SWITCHES CONTACTS STATUS

Case	Contact 89 A	Contact 89 B	Disconnect status
1	OPEN	OPEN	CLOSED
2	OPEN	CLOSED	OPEN
3	CLOSED	OPEN	CLOSED
3	CLOSED	CLOSED	CLOSED

In an open-to-close procedure, the contact 89B opens long before the arcing point, while the 89A remains in the same status until closing. This means that the flags of currents must be assigned as soon as the 89B contact leaves the closed position.

In a close-to-open operation, the relay removes CT currents only when contact 89B reaches its closed position. If that do not occurs, switch will be still considered as closed and currents are kept in the calculations. Finally, during a jammed or short-circuited auxiliary contact, the relay considers the switch closed, so that differential element is secure for this condition.

C. Tripping Logic

Tripping logic must distinguish internal and external faults, recognize the CT saturation and rapidly detect evolving faults. Aiming to do so, the well known tripping logics 1-out-of-1 and 2-out-of-2 are generally used. Initially, the currents in secondary side of CTs are originally mismatched because their transformation ratios are different. To correctly perform the internal calculations in the numerical relay, these values must be standardized by means of a per unit representation, as described in [4].

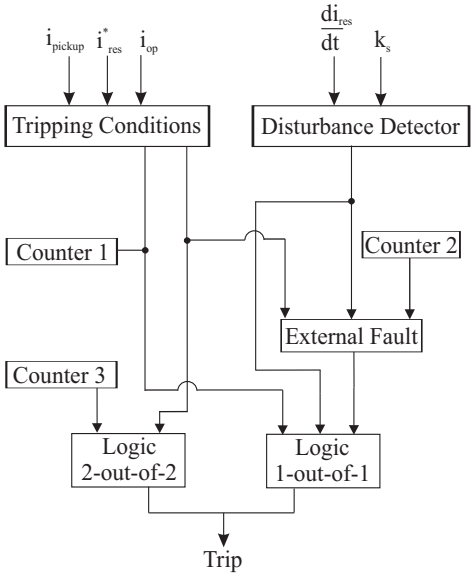

Fig. 3. Tripping logic

As shown in Fig. 3, the normalized input signals of the algorithm are the smoothed restrain current, i^*_{res}, its change rate, di_{res}/dt, and the operation currents, i_{op}. Also, the minimum values of the instantaneous change of i^*_{res}, k_s, in [A/s], as well as the minimum pick-up of operation current, i_{pickup}, are predefined. In the presence of the CT saturation, the original i_{res} can be unstable and the relay might misoperate. To overcome this issue, an stabilizing factor is added in order to obtain a smoothed restraint current i^*_{res} [14], as illustrated in Fig. 4.

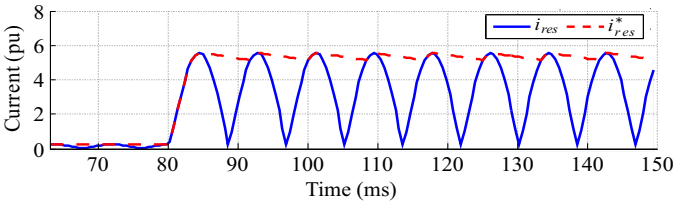

Fig. 4. Comparison between original restraint current i_{res} and smoothed version i^*_{res}.

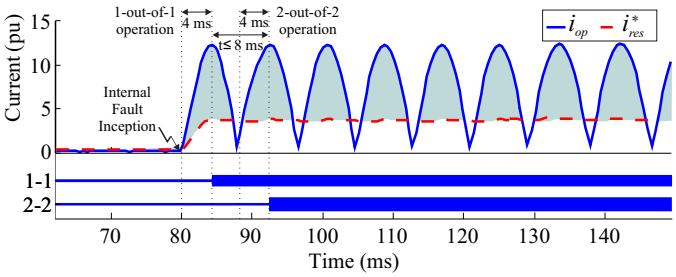

Fig. 5. Tripping conditions for an internal fault

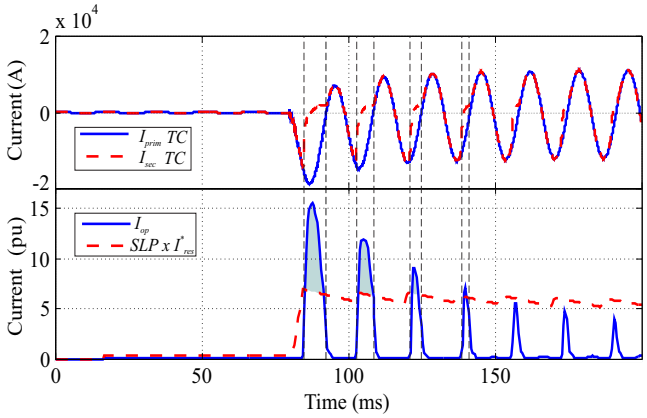

Fig. 6. Impact of CT saturation on i_{op} and i^*_{res}.

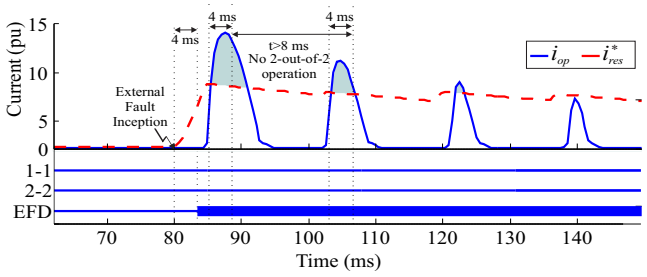

Fig. 7. Evaluation of i_{op} and i^*_{res}. for an external fault with CT saturation

Firstly, the tripping action begins with the detection of the disturbance. This is achieved through the comparison between di_{res}/dt and k_s. After that, it must be verified if the tripping conditions are fulfilled:

$$i_{op} > i_{min} \quad \text{AND} \quad i_{op} > K \cdot i_{res} \ . \tag{3}$$

If the counter 1 confirms these conditions during 4 ms, logic 1-out-of-1 can issue a tripping command. It is important to point out that the count will be reset every time that i_{op} falls below i^*_{res} and will be restarted after i_{op} be again higher than i^*_{res}, as shown in Fig. 5. However, a parallel logic for external fault detection must be implemented before sending the trip command. This type of fault can be verified if i^*_{res} immediately increases after fault inception, while i_{op} remains constant in a negligible value. If the counter 2 counts 4 ms in this condition, the logic 1-out-of-1 enters in a secure mode operation, so its action is blocked during 150 ms.

In this scenario, an additional logic 2-out-of-2 must be ready to operate to avoid the complete vulnerability of busbars in case of a evolving fault takes place, i.e. external to internal faults. In this case, every two consecutive half cycles are evaluated. By using a counter 3, every initial instant, when tripping conditions turn out to be fulfilled, a value is saved. If that occurs in two consecutive half cycles, the interval between these instants must be necessarily lower than 8 ms to recognize the fault as an internal one.

Finally, the CT saturation during an external fault can be recognized in two stages. Firstly, the fast mode operation, 1-out-of-1, is inhibited because of the initial external fault. After a few instants, i_{op} increases rapidly due to saturation. As shown in Fig. 6, i_{op} becomes higher than i^*_{res} during the saturated part of current waveform. The 2-out-of-2 logic remain stable, since this condition is not repeated in two consecutive half cycles within an interval of 8 ms. As the time goes by, the i_{op} lobules will vanish, until it gets below i^*_{res}, as shown in Fig. 7.

III. Simulations and Results

To accomplish the objective of this work, some typical faults were applied in the power system illustrated in Fig. 8. The busbars arrangement is similar to example in section II.A. The objective here is to evaluate the performance of the tripping logics 1-out-of-1 and 2-out-of-2. The disturbance detector (DD) and the external fault detector (EFD) will be activated depending on the fault type. Additionally, a zone protection transfer procedure is described.

A. Internal fault

Applying an AG fault in Bus 1 at 80 ms, the disturbance detector verifies that the i_{op} exceeds i^*_{res} immediately, as seen in Fig. 9. This condition remained for more than 4 ms after the fault inception. As a result, internal fault was immediately recognized and the 1-out-of-1 trip command was sent to the breakers of the network elements connected to the bus 1.

B. External fault

In this case, an external AG fault was applied at 80 ms at the beginning of the transmission line, $TL1$. It is observed in Fig. 10 that, from the fault instant, i^*_{res} increases whereas i_{op} remains with negligible values. The counter verified that this condition remained for more than 4 ms. Consequently, external fault detection logic is fulfilled, thereby no trip command is issued.

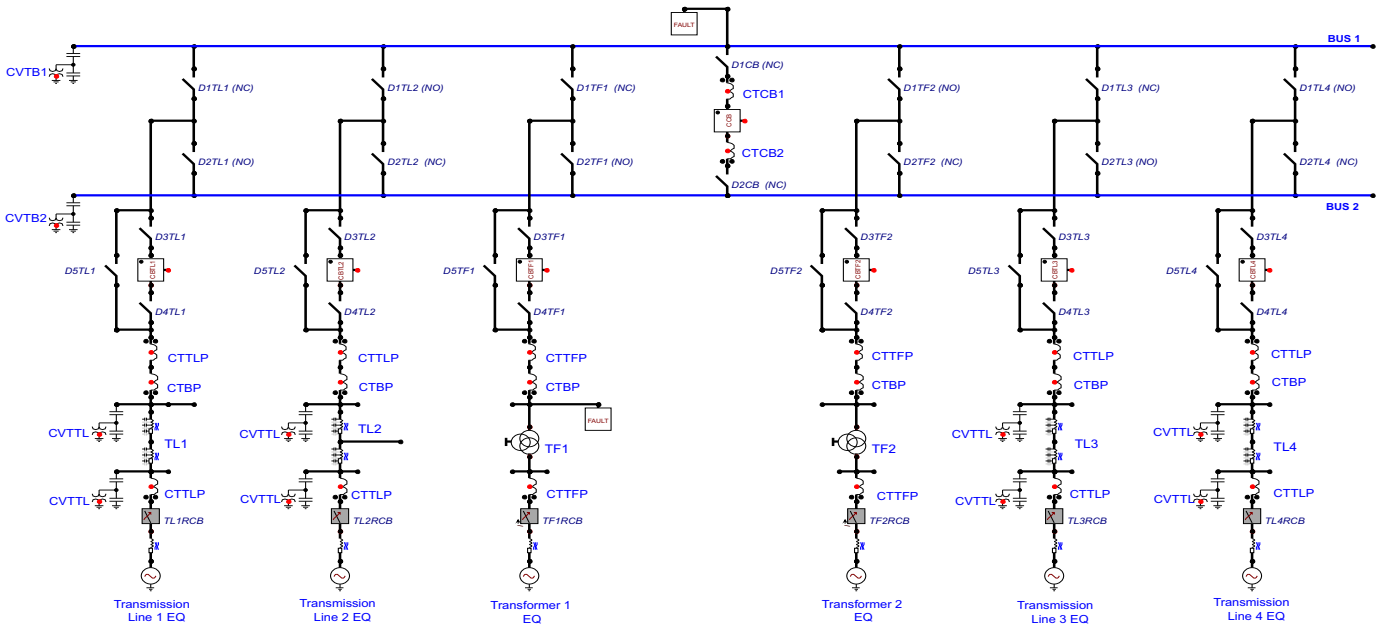

Fig. 8. Single-line diagram of the evaluated double busbar single breaker arrangement

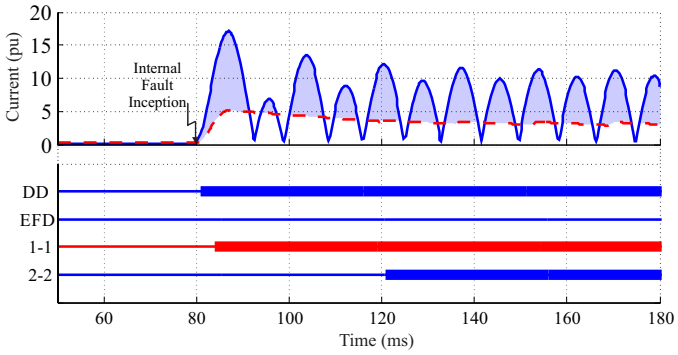

Fig. 9. Internal AG fault in Bus 1 at 80 ms

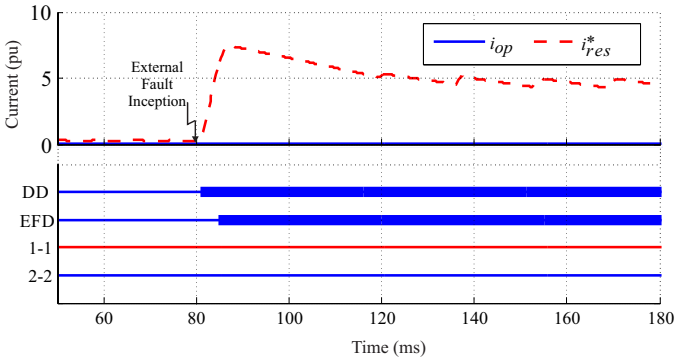

Fig. 10. External AG fault on LT1 at 80 ms

C. External fault with CT saturation

Applying the same fault as the last case, the response of protection system is assessed, considering that *CTBP*, corresponding to breaker *CBTL1* is now saturated. The correct performance of protection algorithm is verified in two stages. Firstly, it can be noted in Fig. 11 that i_{op} increases some milliseconds after the i^*_{res} increment. This conditions are sufficient to recognize the fault as an external one, thus tripping logic 1-out-of-1 is inhibited during 150 ms.

As soon as CT saturates, i_{op} becomes higher than i^*_{res}, satisfying the tripping conditions of Eq. (3). With the fast operation mode blocked, the trip 2-out-of-2 verifies in this case that tripping conditions are never fulfilled in two consecutive half cycles within an 8 ms interval. Consequently, the 2-out-of-2 tripping logic remains stable.

D. Evolving fault with CT saturation

Similarly to last case, the CT installed in the TL1 branch saturates during an external AG fault at 80 ms. However, now it is considered that this fault evolves into bus protection

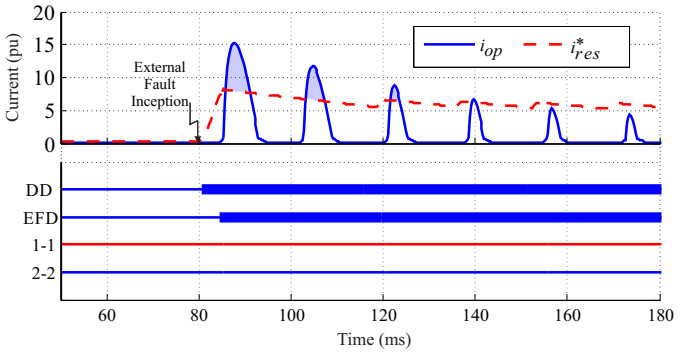

Fig. 11. External AG fault on LT1 at 80 ms, with CT saturation

zone at 110 ms. As aforementioned, during secure mode, the tripping logic 1-out-of-1 is blocked during 150 ms. The new concern is the correct operation of the tripping logic 2-out-of-2 to deal with the internal fault.

The logic 2-out-of-2 requires that tripping condition be accomplished for two consecutive half cycles, within a 8 ms interval. Nevertheless, it can be observed in Fig. 12 that the

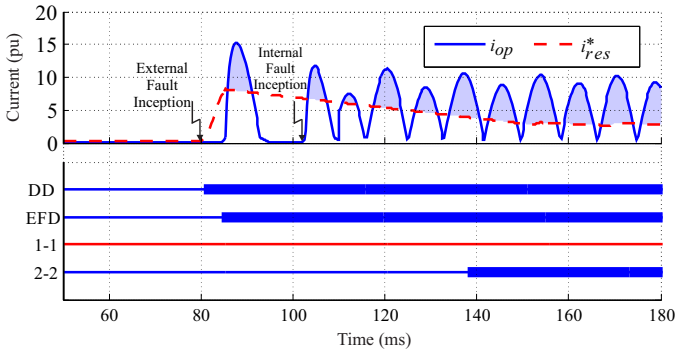

Fig. 12. Evolving fault on TL1 branch

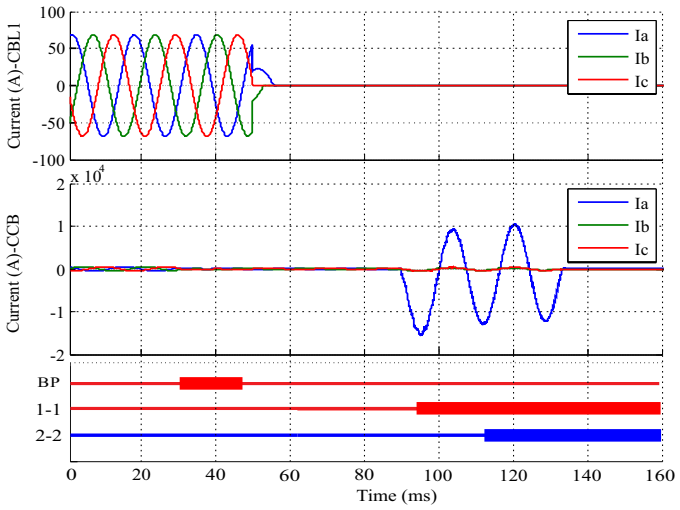

Fig. 13. Response of protection system in front of breaker substitution busbar parallelism logic

trip signal is sent in almost 138 ms.

The lobules size of i_{op} varies according to the decaying DC component, which in turn depends on the inception angle. On the other hand, the decaying time constant of i^*_{res} delays the trip sending signal. In order to overcome this problem, the slope of i^*_{res} could be reduced, but it could also cause i_{op} to be higher than i^*_{res} too fast, causing the rapprochement between the lobules of i_{op} when external fault occurs, i.e. the relay misoperate. Therefore, one can realize a compromise between the operation speed of logic 2-out-of-2 and the security to avoid false trip during external faults with CT saturation.

E. Breaker substitution procedure

In this case, a circuit breaker substitution procedure is simulated in ATP in order to show the application of busbar parallelism logic, as well as the transference of protection zone of the bay connected to the breaker. In order to do so, it was considered that the circuit breaker CB1 must be substituted, such that the tie breaker must protect this bay. For the sake of simplicity, the duration of the procedures was reduced to a millisecond scale.

As observed in Fig. 13, the parallelism condition occurs during the simultaneous closure of the selector switches for both buses. After that, the bypass switch is closed and the breaker is opened, as well as their disconnect switches. Now, the tie breaker will automatically assumes the role of protection of the bay TL1. In this way, when the fault occurs in 90 ms, the trip 1-out-of-1 is sent after approximately 4 ms and the complete extinction of the fault occurs 2 cycles later.

IV. Conclusion

In order to ensure the stability of power systems, bus protection plays an important role. This paper presented the principles of microprocessor-based bus differential protection by using instantaneous values of currents. Specifically, traditional 1-out-of-1 and 2-out-of-2 protection logics was tested in a 230 kV power system by applying typical faults. It was exhibit how the success of this algorithm in a variable busbar arrangement depends on the correct design of an additional dynamic zone selection logic. The results show the applicability of this technique in dynamic busbars topologies, as well as its ability to recognize external faults, the CT saturation, as well as common technical procedures in busbars.

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References

[1] K. Behrendt, D. Costello, and S. E. Zocholl, "Considerations for using high-impedance or low-impedance relays for bus differential protection," *IEEE 63rd Annual Conference for Protective Relay Engineers*, pp. 1–15, March 2010.

[2] C. Martin, S. Chase, T. X. Nguyen, D. J. Hawaz, J. Pope, and C. Labuschagne, "Bus protection considerations for various bus types," *69th Annual Georgia Tech Protective Relaying Conference*, April 2015.

[3] G. Ziegler, *Numerical Differential Protection, Principles and Applications*, 4th ed. Berlin: Publicis Corporate Publishing, 2011.

[4] H. J. A. Ferrer and E. O. Schwitzer, *Modern solutions for protection, control, and monitoring of electric power systems*. Pullman: Schweitzer Engineering Laboratories, 2010.

[5] S. Wang, X. Dong, and S. Shi, "A novel busbar protection scheme based on wavelet multi-resolution signal decomposition," *10th IET International Conference on Developments in Power System Protection*.

[6] M. A. Ibrahim, *Disturbance Analysis for Power Systems*. New York: Wiley, 2012.

[7] W. A. Elmore, *Protective Relaying, Theory and Applications*, 2nd ed. New York: Springer, 2008.

[8] S. Song and G. Zou, "A novel busbar protection method based on polarity comparison of superimposed current," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 1914–1922, Aug 2015.

[9] H. Gao, G. Zou, and M. Xiang, "A fast busbar protection technique based on travelling wave," *IEEE Power and Energy Society General Meeting*, pp. 1–6, July 2012.

[10] B. L. Qin, A. Guzman, and E. Schweitzer, "A new method for protection zone selection in microprocessor-based bus relays," *IEEE Transactions on Power Delivery*, vol. 15, no. 3, pp. 876–887, July 2000.

[11] A. Guzmán, B. L. Qin, and C. Labuschagne, "Reliable busbar protection with advanced zone selection," *IEEE Transactions on Power Delivery*, vol. 20, no. 2, pp. 625–629, Apr 2005.

[12] IEEE, *Guide for protective relay applocations to power system buses*. New York: IEEE Power and Energy Society, 2009.

[13] C. Labuschagne, N. Fischer, and B. Kasztenny, "Simplifying and improving protection of temporary and unusual bus configurations with microprocessor-based relays," *67th Annual Georgia Tech Protective Relaying Conference*, May 2013.

[14] A. Kumar and P. Hansen, "Digital bus-zone protection," *IEEE Computer Applications in Power*, vol. 6, no. 4, pp. 29–34, Oct 1993.