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# A 320 Gbps board level Data Sourcing System FPGA Design

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**Abstract**. The evolution of FPGA Multi Gigabit Transceivers (MGT) brought opportunities for data formatter and data acquisition projects in several areas. The newer FPGA families are capable to handle Gigabit I/Os implemented over high speed serial link protocols and becoming the future downstream processors. The digital systems created for that purpose need to be reliable and synchronous between dozens of channels and boards. In order to have instruments to test these projects, this work implemented an emulator that is capable to produce data synchronized in 40 channels up to 8 Gbps each. This system was built using the Pulsar 2b, a custom ATCA FPGA-based board designed by Fermilab, to be a scalable high speed link processor system. The results showed that the system is able to provide data, and to measure synchronization, latency and bit error rate of the MGTs.

**Keywords**. Emulator System, ATCA, FPGA, High Speed Serial Link Protocol.

## 1 Introduction

The newer FPGA families are able of handling several Gigabit I/O channels implemented over high speed serial link protocols [2] [8] [9], operating in high internal clock frequencies [4] and also of serving as future downstream co-processors due the its internal DSPs resources [6]. Any algorithm can be parallelized and accelerated by a FPGA, becoming faster than a standard DSP processor [11].

The evolution of FPGA Multi Gigabit Transceivers (MGT) brought opportunities for data formatter and data acquisition (DAQ) projects in several areas. Some examples

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are: power systems [11], aerospace instrumentation [1], climatology instrumentation [5], network computers [4], physics instrumentation (HEP) [2], among others.

The digital systems created for DAQ and formatting need to be reliable and synchronous between dozens of channels. In order to ensure the synchronization, the latency of multiple links should be similar and the digital system in the FPGA should allow the insertion of synchronization signals [3]. Thus, to synchronize multiple boards, the electronic devices should receive the same synchronization signals.

A DAQ Systems under development steps needs an emulator to act as data source and to help the debugging. The FPGA systems are capable of emulating the data input according to the hardware capability [10].

In order to have instruments to test these projects, this work implemented an emulator, the Data Sourcing System (DSS), that is able to produce data synchronized in different channels with total bandwidth up to 320 Gbps.

The DSS was implemented and tested using the Pulsar 2b, a custom Advanced Telecommunications Computing Architecture (ATCA) FPGA-based board designed by Fermilab to be a scalable high speed link processor system [12]. The Pulsar 2b Board has as core a FPGA with 40 Multi Gigabit Transceivers (MGT) connected to a Rear Transition Module (RTM). In this work, we focus in the implementation and test of these RTM links. The development of the FPGA Design described in this work used the ATCA infrastructure documented previously at [13].

The tests performed used two Pulsar 2b boards. One perform the emulation of data, and the other record the data received to check latency, bit error rate and synchronization. The management and debug is performed using Integrated Logic Analyzers (ILA) or IPbus.

The results shown that the system is able to provide data and, to measure synchronization and signal integrity, latency and bit error rate of the MGTs. The boards are accessible by python scripts and scalable to multiple boards scenario.

This work is organized in sections as follows. Section 2 presents the Pulsar 2b board and describes the DSS FPGA design. The tests and results performed are shown at Section 3. Finally, Section 4 concludes the work.

## 2 Data Sourcing System

The Fermilab R&D team designed the Pulsar 2b, illustrated at Figure 1, for applications that require a full-mesh ATCA backplane to share data inside the ATCA shelf. Moreover, the board have massive I/O capabilities through RTM boards with a maximum 400 Gbps [12].

The core of the board is a Virtex-7 FPGA, model XC7VX690T-FFG1927-2, which contains 80 MGTs available for high speed serial communication. The distribution of these transceivers is listed bellow:

**FMC Mezzanines** 12 MGTs, 3 per mezzanine, connected through FMC connector.

**RTM MGTs** 40 MGTs to QSFP+ connectors for cooper or optical fiber cables.

**Backplane** 26 MGTs, 2 per each of the other 13 boards inside the shelf.

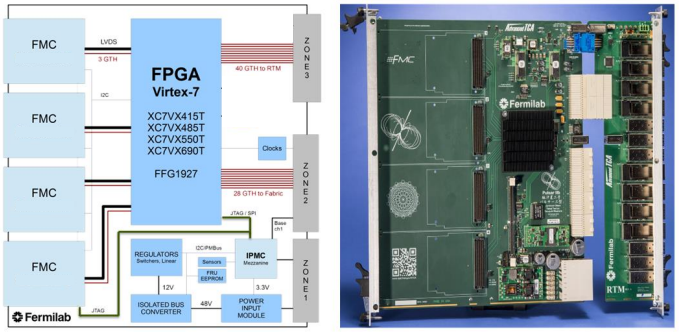


Figure 1: Left: Pulsar 2b Block Diagram. Right: Photo of Pulsar 2b Board with RTM. Source: Adapted from [12].

The ATCA backplane also provides lines to share signals through all physical slots. Those signal lines can send/received clock or data through the ATCA backplane. The DSS FPGA design uses this Pulsar 2b resource for synchronization purpose.

## 2.1 Data Sourcing System FPGA Design

The DSS is composed by two similar designs, the DSS Sender and DSS Receiver, which have roughly the same elements. The DSS Sender, illustrated at Figure 2, was implemented with the following elements:

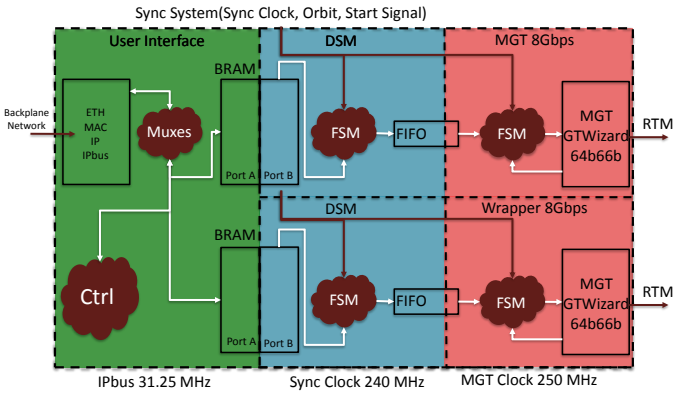


Figure 2: DSS Sender FPGA Design.

**Sync system** Process capable to either emulate or use a external input of signals to be propagated in the ATCA backplane. The signals used should be 240 MHz Sync clock used to synchronize the internal logic of the DSS design, and a periodic flag (11 MHz) used to reset MGTs and FIFOs, and an asynchronous start signal, controlled by the user. The combination between those signals are used to synchronize the boards in the same ATCA shelf.

**User Interface** It provides a direct connection between the computer and the FPGA memory blocks. The TCP/IP network is provided by a MGT connected through the ATCA backplane to a ATCA Switch. It allows to read and write data to the RAM blocks at the FPGA board at 31.25 MHz rate. The DSS is compatible with the IPbus protocol [7]. It is also possible to use W/R operations to set and get parameters from the board, like reset signals, change tuning, measure BER and latency, among others.

**DSB** The Data Sourcing Board is composed by the Remote Control system, 40 Groups of Data Sourcing Module (DSM), FIFOs and MGT Serial Link Protocols, despite Figure 2 illustrated only two of the 40 groups.

**DSM** Subset of memory reserved for each MGT channel. Each module has a Dual Port Block RAM of 4k x 32 bits memory. One port is used as User Interface clock domain while the other deals with the sync clock. The Sender side needs to receive a start signal from Sync System to transfer the data from the memories to the FIFO.

**FIFO Manager** The FIFO manager is located between the DSM and the MGT Channels. It also interfaces the clock domains of Sync Clock and MGT Clock. The FIFO size should be equal to the DSM size.

**MGT** It is responsible for flowing data in a serial link protocol through each one of the RTM links. There are a few protocols capable to perform this task, in this work the Xilinx GT Wizard Aurora 64b/66b was used. The data rate for this work is 8 Gbps per MGT and the clock that drives the internal parallel logic is 250 MHz.

The difference between DSS Sender and Receiver is the data flow: the sender receives the user data input through IPbus and, using the sync signals, can (re)load data from BRAMs to FIFOs and sent to MGTs. The DSS Receiver receives the data sent, (re)load the FIFO and record them in the BRAMs. After this process, the user can read the data received, measure BER, latency and can rearm the system to run the scenario again.

## 3 Board Level Tests

The Data Sourcing board level setup uses two Pulsar 2b boards connected by 10 QSFP+ optical cables in the RTM. One of the boards has its FPGA programmed with DSS Sender design and the other with the Receiver design. In the Figure 3, there is a Cumulative Distribuition Function (CDF) of the Bit Error Rate (BER) measured by DSS at receiver side. The measurement was performed in 40 channels, operating at 8 Gbps each, and the sampling in the order of 1 Tbits per channel. The CDF shows that 80% of the channels presents BER lower than $10^{-8}$. The measurement can be used by the application to identify the link integrity and find solution to improve it. In this work, proper changes to improve link performance were not done.

The user can load the data in the Sender design via IPbus using python scripts on a PC. A file can be used to load data samples to be transmitted at the 40 MGTs. In this

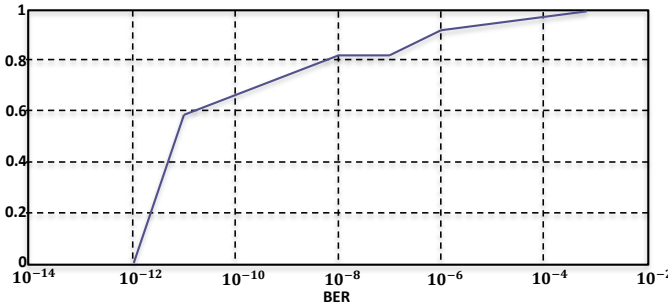


Figure 3: CDF BER Board Level.

work, test data was used. After loading the data, the user can start the scenario using the sync start signal connected with Virtual Input Output(VIO). The start signal needs to be sent when the user wants to transfer the data from Data Sourcing Modules. The reading process at Data Sourcing Receiver is important to check if the data received is the same as the sent one. The receiver, which is in the same ATCA Shelf, should use it as a marker for latency measurements. The logic used in the sync signals relation is illustrated at Figure 4. The left side shows how the Receiver side, by receiving the same sink signals, can measure the latency of the MGT

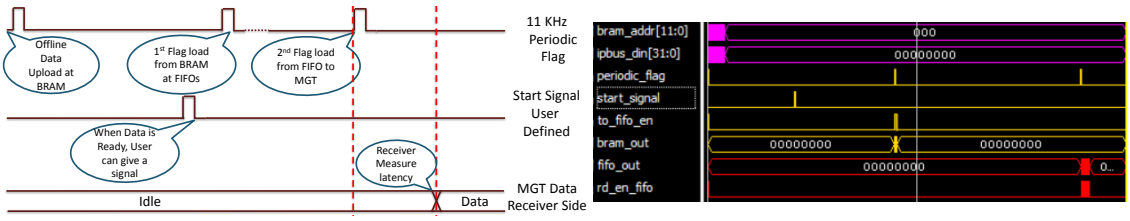


Figure 4: Left: Synchronization Signals. Right: Waveform Simulation of DSS Sender Side.

The latency is measured at Receiver Side in different MGT data speed rates, what is illustrated by Figure 5. The latency is related to the MGT clock frequency, which is generated by the GTH Wrapper based on the speed desired.

The latency jitter, which influences the alignment of all links, is 4 clock cycles long. The jitter is caused by the 64b/66b enconding gearbox pauses in TX and RX with 2 clock cycles in each one. The jitter effect can also be measured by the latency ILA instead the allignment one.

## 4 Conclusions

The DSS can be applied as an emulator of any DAQ or Data Formatter project to aid the debugging process. In fact, it has been used at Fermilab R&D of High Energy projects to emulate physics experiments data input.

Data Sourcing has shown features that makes the system be of generic usage. There

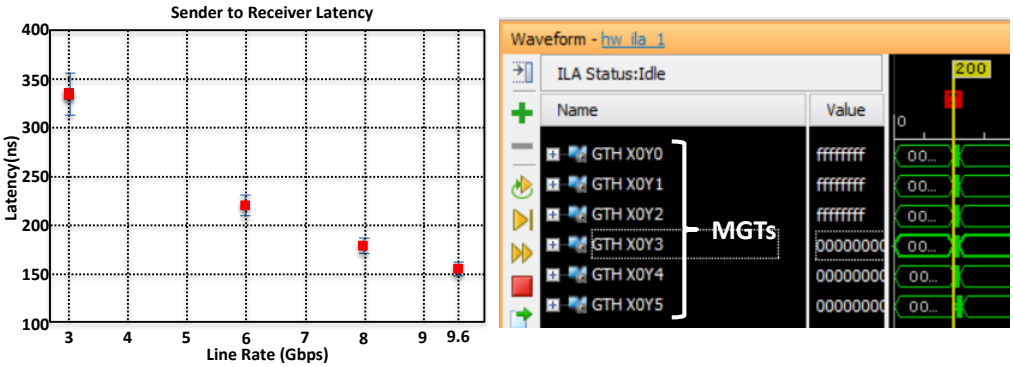


Figure 5: Left: Wrapper Latency. Right: Data Received Allignment

are 131 kbits available in BRAM to be written or read by the system. The memory size can be increased if needed.

The Sync System ensures the synchronization of all links with reasonable alignment ($\pm$20 ns). Considering that the signals propagate through the backplane, it can be applied for multiple boards scenario. A simple reset can be performed with the User Interface to rearm the system. Moreover, Data Sourcing performs some advanced functions, such as latency measurements, BER measurements and tuning parameter settings.

Future work relies in shelf level tests using 10 boards, besides increasing the links integrity for a 3.2 Tbps low-level error communication.

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