DEVELOPMENT OF EFFICIENT 1U CUBESAT ELECTRICAL POWER SUPPLIES - BOOST CONVERTER OPTIMIZATION

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Abstract— Since early 2000 a nano satellite class called CubeSat is been used by universities, companies and military organizations to explore the space, developing researches and validating new space technologies. The physical dimension of a one unity (1U) CubeSat, 10 cm each edge, imposes a low power generation in space orbit. Thus, the development of power electronics for space applications demands high efficiency with size, volume, mass and losses reduced simultaneously. Those limitations force the electrical power supply (EPS) and its power converters efficiencies higher than 90%. This paper presents a design methodology for boost power converters in order to improve efficiency, to reduce volume and mass for 1U CubeSat EPS. Theoretical and practical results validated the design methodology and the optimal design reached efficiencies higher than 90% respecting the 1U CubeSat constraints.

Keywords— CubeSat, electrical power supply, DC-DC power converters

Resumo— Desde os anos 2000 uma classe de nano satélites chamada de CubeSat vem sendo utilizada por universidades, empresas e organizações militares para a exploração espacial, desenvolvendo pesquisas e validando novas tecnologias espaciais. A dimensão física de um CubeSat 1U, 10 cm de aresta, impõe uma baixa geração de energia elétrica na órbita espacial. Assim, o desenvolvimento de eletrônica de potência para aplicações espaciais demanda alto rendimento com tamanho, volume, massa e perdas elétricas reduzidas simultaneamente. Ademais, essas limitações forçam a fonte de alimentação (EPS) e seus conversores de potência a rendimentos superiores a 90%. Portanto esse trabalho apresenta uma metodologia de projeto para conversores boost síncronos de modo a aumentar o seu respectivo rendimento, reduzir o volume e a massa para a aplicação de uma fonte de alimentação para um CubeSat 1U. Resultados teóricos e práticos validaram a metodologia e o design ótimo alcançou o rendimento superior a 90% respeitando as limitações de projeto impostas pelo nanossatélite.

Palavras-chave— CubeSat, fontes de alimentação, conversores de potência CC/CC

1 Introduction

CubeSats are small satellites with a cubic shape where a standard unit measures 10 cm each edge(Munakata, 2009). This satellite topology has been created to provide more integration among students, professors and researchers in every space mission step; reduction of costs; simplicity in the design; use of radio amateur frequency band and space qualification of the future small payloads (Munakata, 2009)(Puig-Suari et al., 2001).

Fundamentally, a satellite is composed by different systems like the on-board computer (OBC), EPS, sensors, solar panels, telecommunication, and payloads to develop a specific space mission. Thus, in this work, it is given attention to the CubeSat EPS, which is the system responsible to generation, storage, conditioning, control and supply of electrical power to the satellite (Patel, 2004), Figure 1.

Electrical power generation in a CubeSat is made by photovoltaic conversion from the solar primary source through 12 solar panels attached to its six faces. By the way, a low electrical power generation is available to this nanosatellite topology due to the small solar cell coverage area, which in a 1U standard CubeSat is equal to 362.16 cm^2.

Additionally, other restriction to power generation is the ratio between the eclipse time $t_{eclipse}$ and the orbital period T_{orbit} in Low Earth Orbit (LEO), which is approximately 35 minutes of sun absense in 96 minutes of orbital period.

EPS makes an interface between the solar cells and all the electronics systems like the OBC, payloads and sensors. Therefore, this work presents a design methodology for a 1U CubeSat EPS comparing different inductors and semiconductors technologies, switching frequencies, current ripple and current density. In this project has been used power consumption and power generation data from Brazilian CubeSat, NANOSATC-BR1 (Programa NANOSATC-BR Desenvolvimento de CubeSats , 2014). Additionally, constraints of size, mass, losses and temperature for each power converter are taken into account in the optimal design methodology.

Numerous power converter optimization design methodologies were presented in literature where (Sartori et al., 2009) and (Beltrame et al., 2013) have increased up converters efficiencies up to 99.0 %. In (Lefranc et al., 2012) is presented a buck converter optimization process called presizing, where a pareto front establishes the maximum efficiency to be reacheable by the power

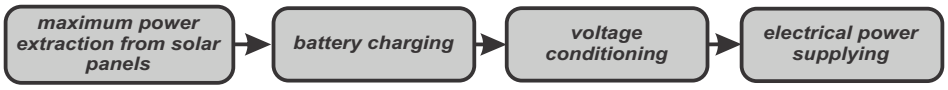

Figure 1: Electrical power processes executed by the CubeSat EPS

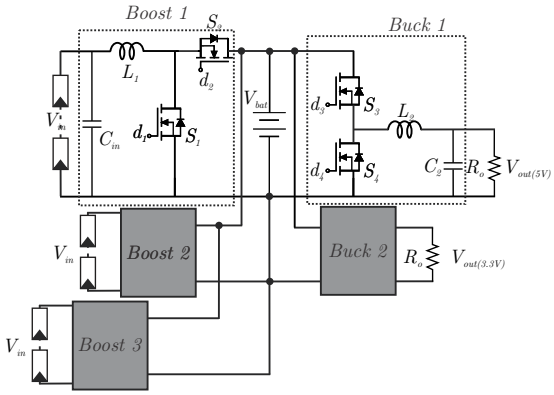

Figure 2: Proposed EPS topology

converter. Also in (Zidar et al., 2016) is presented a review of different optimization methods to achieve a optimal sitting and sizing of energy storage systems.

2 Electrical Power Supply

2.1 Power Electronics into CubeSats

Explained in previous section, the interface between solar panels and batteries and the interface between batteries and regulated bus (5 V and 3.3 V) is made commomly by different power converters. Therefore commercial and scientific papers related to 1U CubeSat EPS were analyzed looking at power converters topology and its efficiency. Thus, SEPIC power converter, buck-boost and boost power converters usually are used as battery chargers in EPS (GomSpace NanoPower Systems, 2016)(Clyde Space Company, 2016)(Crystal Space, 2015)(Blue Canyon Technologies , 2016)(Singh et al., 2015). Also a linear regulator is developed in (PUMPKIN INCORPORATED, 2012). Moreover was observed that power converter efficiencies are close to 90% in this kind of application due to small output power and relation between input and output voltage.

The power conditioning procedure is commomnly made by buck power converters with efficiencies close to 95%.(GomSpace NanoPower Systems, 2016)(Clyde Space Company, 2016)

In this work synchronous boost converters are studied and developed in order to achieve a good performance and higher efficiency in comparison with conventional power converters, due to substantial losses in power diodes. As presented in previous works (Badstuebner et al., 2010) (Kolar and Minibock, 2012) have raised power converters efficiency has up to 99.2 % when the power diode was changed by a MOSFET in a synchronous configuration. Moreover in CubeSat topology all the systems have to be compact and efficient due to the spatial distribution inside the satellite. Hence, EPS volume and mass constraints are specified looking to NANOSATC-BR1 EPS parameters, where the specifications are presented in Table 1 disregarding the 18650 Li-ion batteries volume and weight.

Table 1: EPS constraints of volume/size and mass

Parameter	Value
EPS volume $[cm^3]$	184.27
EPS weight $[g]$	150.00
power converter volume $[cm^3]$	36.00
power converter weight $[g]$	30.00
EPS input voltage [V]	$2.50 - 5.00$
battery voltage [V]	$6.00 - 8.40$
maximum boost output power [W]	3.00

The space mission success necessarily depends on the availability of electrical power into the satellite. Hence, EPS power converters have to be reliable and designed to support satellite maximum power generation and the peak power consumption. NANOSATC-BR1 data information has served as reference into power consumption and generation, Table 2, where the duty cycle term is the relation between the operational time in space orbit.

2.2 Power losses in power electronics

Comprehend the behavior and power losses in every electronic and magnetic component are necessary steps to define an optimal design in power electronics devices. So, this section describes the losses modelling of inductor, semiconductor switches and capacitor for a synchronous boost power converter.

2.2.1 Inductor losses

Inductor losses are result of Joule effect in the cooper windings and magnetic flux variation within magnetic material. Core losses in every switching period are given in (Liu et al., 2002) by (1).

Table 2: NANOSATC-BR1 power consumption

subsystem	current(related to 7.5V)[A]	power[W]	duty cycle[%]	energy consumed[$W.h$]
EPS	0.033	0.2497	100	0.2500
Antenna	0.005	0.3997	100	0.0400
OBC	0.031	0.2310	100	0.2300
TRXUV RX	0.030	0.2250	100	0.2200
Housekeeping	0.020	0.1500	100	0.1500
Payloads	0.031	0.2317	100	0.2300
TRXUV TX	0.105	0.7875	0.3	0.0023
TOTAL	0.255	1.9149	-	1.13

$$\frac{P}{V} = a\left(\frac{\Delta B^m}{(2t_{on})^n}\cdot\frac{t_{on}}{T_S} + \frac{\Delta B^m}{(2t_{off})^n}\cdot\frac{t_{off}}{T_S}\right) \quad (1)$$

where t_{on} is the interval when the switch is on; t_{off} is the interval when the switch is off; ΔB is the magnetic flux; a, m and n are the Steinmetz coefficients; T_S is the switching period and V is the core volume;

Additionally, conduction losses in windings are the effect of AC and DC electrical resistances. Thus, DC resistance is shown in (2) (Rashid, 1999) and the AC resistance, which depends on the turns number N, cooper permeability μ, harmonic frequency f, conductor diameter d, distance between centers adjacent conductors td, and turn average length l_{esp} is not considered in this work.

$$R_{DC} = \frac{\rho\cdot l}{A} \quad (2)$$

with ρ the material electrical resistivity; l the conductor length; A the conductor cross-section area;

Hence, simplified conduction losses in cooper windings are expressed in (3).

$$P_{cond} = R_{DC}\cdot i^2_{L(rms)} \quad (3)$$

where $i_{L(rms)}$ is the rms magnetic current;

2.2.2 Semiconductor losses

Semiconductor switches are affected by conduction and switching losses (Mohan, 2003). Conduction losses, (4), causes heat wich elevates the semiconductor junction temperature, changing the electrons mobility and consequently amplifying power losses due to drain to source resistance $R_{ds(on)}$ raise.

$$P_{cond} = R_{ds(on)}\cdot I^2_{rms} \quad (4)$$

When the power diode is replaced by a semiconductor switch in a synchronous configuration a dead time between the S_1 and S_2, Figure 2 switch must be ensured. This limitation time protects the switches against a shoot through phenomenon, which elevate power losses in semiconductors and can damage the component by reason of a current spike. When the synchronous switch is turning off, during the dead time an intrinsic diode conducts electric current causing losses (5) (Christian and Olivier, 2012). The diode current will be reduced to zero but the minority carriers forces the reverse conduction until the total recombination with oposite electric charges. This recombination process will generate losses as presented in (6).

$$P_{diode} = V_d\cdot I_{sd}\cdot t_{dead}\cdot f_{sw} \quad (5)$$

with I_{sd}, reverse drain current presented by the intrinsic diode; V_d, voltage through the diode;

$$P_{rr} = V_{out}\cdot f_{sw}\cdot Q_{rr} \quad (6)$$

A synchronous configuration in power converters imposes a gate driver device which is responsible to adequate gate to source voltages for both semiconductor switches. Thus gate driver losses are generated due to gate charge of the MOSFET Q_g and proportional to switching frequency (7)(Christian and Olivier, 2012).

$$P_{gate} = Q_g\cdot V_g\cdot f_{sw} \quad (7)$$

When semiconductor switches turns on the output charge Q_{oss} is charged consequently generating additional power losses (8) (Jauregui et al., 2011) (Christian and Olivier, 2012).

$$P_{Qoss} = V_{out}\cdot f_{sw}\cdot Q_{oss} \quad (8)$$

Furthermore an overlap of $I_{S1(RMS)}$ and V_{dS1} caused when the semiconductor S_1 is switching on and switching off is presented in the power converter (Xiong et al., 2009).

$$P_{sw} = \frac{1}{2}\cdot f_{sw}(V_{dS1}\cdot I_{S1(RMS)})(t_{on}+t_{off}) \quad (9)$$

with t_{on} MOSFET turn-on and t_{off} the MOSFET turn-off;

2.2.3 Capacitor losses

Input capacitors are necessary in photovoltaic application to filter the input voltage and minimize the voltage ripple to extract the maximum power from solar panels. On the other hand power losses

are generated by Joule effect, where in (10) is shown a relationship between the electrical current and the capacitor internal resistance R_{ESR}.

$$P_{cap} = i^2_{cap(RMS)} \cdot R_{ESR} \tag{10}$$

3 Design Methodology

In power electronics three important variables have to be taken into account to design a DC/DC power converter, which are switching frequency $f_{sw}[kHz]$, inductor current ripple $\Delta I[\%]$, and current density $J[A/cm^2]$ which define the power converter operational point. With the increase of ΔI and f_{sw} an inductor volume minimization is achieved. Furthermore, the current density is directly related to cooper area in the inductor windings and a minimization of this therm reduces (2) and consequently cooper losses (3). Also environmental and junction temperature increment in semiconductor switches can amplify its power losses.

Thereby, the presented methodology consist in a matrix of multiple designs with different parameters, making a big computational sweep in order to find the optimal design which reach all the 1U EPS CubeSat constrains of volume, mass and efficiency. Thus, an algorithm based on multi objective computational interactions was developed taking into account components models and data acquired from commercial components datasheets. In each operational point is calculated the converter efficiency, volume, mass, magnetic core and cooper winding losses and capacitor losses, presented in Figure 3.

3.1 Inductor design

With a switching frequency, inductor current ripple and current density sweep, different inductors are calculated with optimal characteristics in order to minimize the electrical and magnetic losses. The ideal powder core choice is made in accordance with the energy stored by the inductor, maximum volume allowed for the EPS application and minimal losses and the converter minimal inductance $L_{min(boost)}$ is calculated in accordance with (12) to assure a specific current ripple ΔI_{max}, derived from (11).

$$v_L = L\frac{di_L}{dt} \tag{11}$$

$$L_{min(boost)} = \frac{D \cdot V_{in}}{I_{pk} \cdot \Delta I_{max} \cdot f_{sw}} \tag{12}$$

where D is the duty-cycle, calculated in (13).

$$D = 1 - \frac{V_{in}}{V_{out}} \tag{13}$$

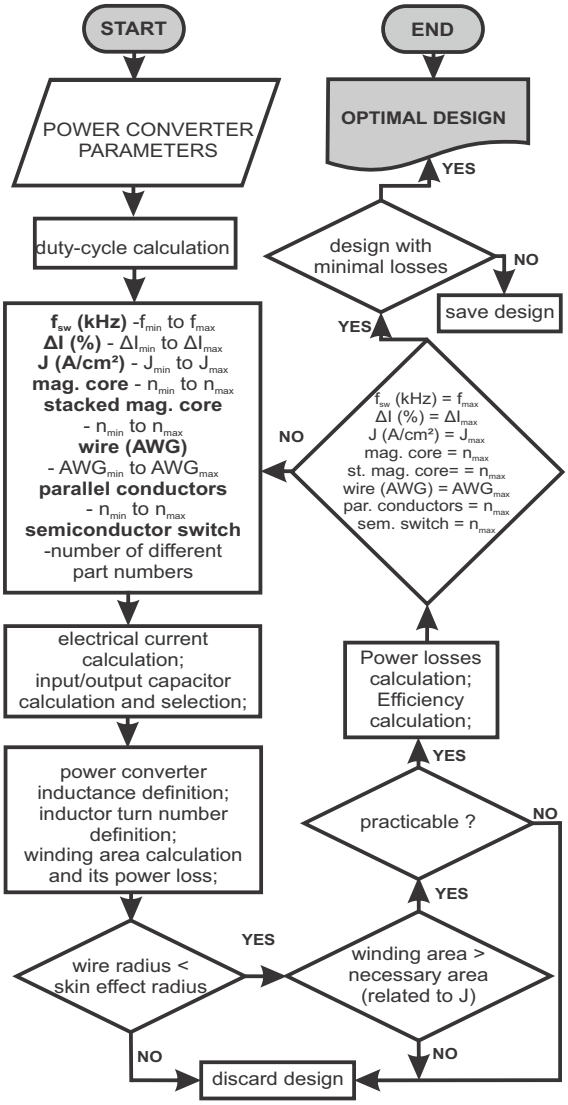

Figure 3: Multi objetive computational interactions executed in the optimal design methodology algorithm

3.2 Semiconductor selection

In this work was investigated commercial semiconductor switches with low $R_{ds(on)}$ and gate-source capacitance C_{gs} in order to minimize the semiconductor losses.

3.3 Input capacitor design

To assure a maximum input voltage ripple ΔV_{max} the input capacitor C_{in} has to be calculated as shown in (14), derived from (15).

$$C_{in} = \frac{D \cdot (i_{in})}{\Delta V_{max} \cdot f_{sw}} \tag{14}$$

$$i_C = C\frac{dv_C}{dt} \tag{15}$$

4 Results

In order to validate the proposed methodology a physical prototype was developed, Figure 5, and results have been carried out with Yokogawa Power Analyzer WT1800. The optimal design presented efficiency of 94.38% in software simulation and 94.078% in physical prototype, Figure 6. Furthermore other power converter characteristics are shown in Table 3. Additionally in Figure 4 is shown where the optimal desing is located in a wide range of switching frequency and current ripple values considering $J = 270\ A/cm^2$.

Table 3: Synchronous boost converter with optimal design

optimization variable	optimal value
switching frequency : f_{sw}	$14kHz$
current ripple: ΔI	40 %
current density: J	270 A/cm^2
converter efficiency: η_{boost}	94.38%
converter volume:	2.7 cm^3
converter weight :	19.2 g
converter inductance: L_{boost}	354.46 μH
input capacitance: C_{in}	530 μF
inductor turns number :	54
cooper wire classification:	AWG 25
conductors in parallel:	2
core part number:	77380
stacked mag. core:	2

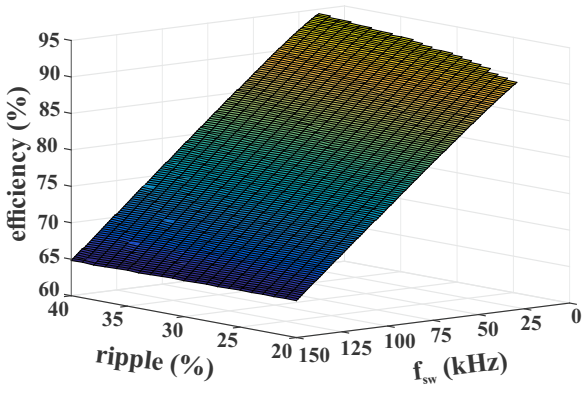

Figure 4: Optimal boost converter efficiency

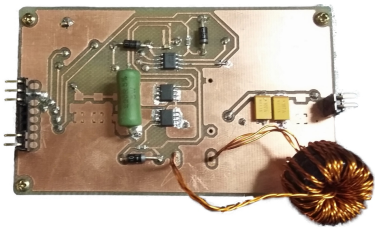

Figure 5: Synchronous boost converter prototype

The optimal design methodology have been carried out considering the converter input voltage equal to $V_{in} = 3.5\ V$. This value was defined

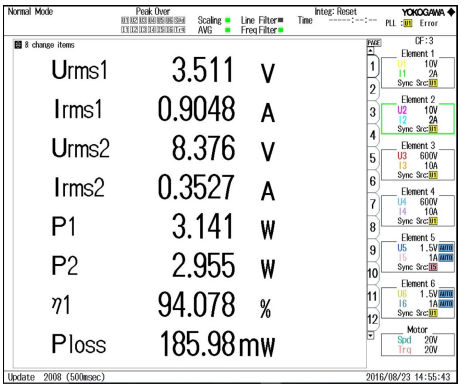

Figure 6: Optimal design - practical results. $V_{in} = 3.5\ V$, $V_{out} = 8.376\ V$, $P_{in} = 3.141\ W$, $P_{out} = 2.955\ W$, $efficiency = 94.078\%$

in previous analysis with NANOSATC-BR1 EPS data telemetry. However, after the development of tests in the physical prototype was observed a substantial difference among boost converter efficiency η_{boost} with varied input voltages V_{in}. When V_{in} is increased also the η_{boost} steps up, as shown in Figure 7. Accordingly to these results further studies have to be conducted in order to define the weighted mean V_{in} in space orbit to maximize the energy stored in batteries.

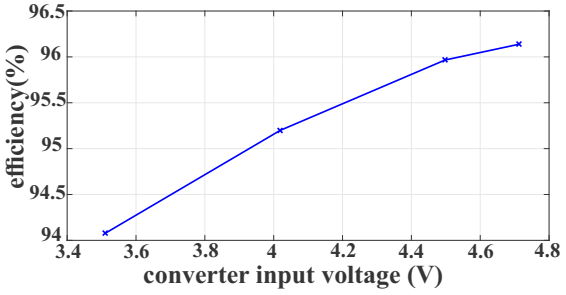

Figure 7: Relation between power converter input voltage V_{in} and efficiency η_{boost} with nominal output load ($P_{out} = 3\ W$)

5 Conclusions and Future Challenges

In this paper an optimization design methodology of synchronous boost converters for 1U CubeSat EPS is given in detail. Optimal design was achieved with multi objective computational interactions and results have been acquired by mathematical simulation and experimental tests, validating the proposed methodology. Efficiency improvement at rated power has been achieved for the synchronous boost converter, with 94.078 % ($V_{in} = 3.5V$) and 96.138 % ($V_{in} = 4.713V$ -solar cell maximum power point). In order to raise the converter efficiency to higher levels new studies have to be conducted in the converter operational

mode (CCM-BCM-DCM); a comparison with conventional power converters using low voltage drop schottky diodes; and the weighted mean V_{in} in space orbit.

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