COMPARISON OF BOOST-BASED NONISOLATED DC-DC CONVERTERS FROM THE EFFICIENCY POINT OF VIEW

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Abstract—In order to define the most appropriate power electronic converter topology for a specific application, several aspects must be analyzed, such as cost, efficiency, size, and volume of the chosen structure. However, this may not be a trivial task in structures with high number of active and passive switches. This work applies the concept of commutated power to five step-up dc-dc boost-type converters, that are the classical boost converter, the quadratic boost converter and dc–dc boost converters based on the three-state switching cell (3SSC) and voltage multiplier cells (VMCs) with one, two and three VMCs. Thus the power commutated by the inductor and semiconductors in the aforementioned converters is analyzed in order to establish qualitative criteria that allow determining which type of arrangement is the most adequate one for a given operating point. Besides, it aims to validate the theoretical assumptions by calculating conduction and switching losses in the semiconductor devices, while PSIM® simulation software is used only to obtain the commutated power curves. Finally, the performance of each one of the converters is evaluated from the energy efficiency point of view.

Keywords **–** commutated power, dc-dc converters, semiconductor devices, high voltage gain converters, switching losses.

1. Introduction

Recently, high-voltage step-up nonisolated dc-dc converters have drawn significant attention from researchers in the field of power electronics. The proposed approaches have been specifically focused on specific issues, which include the achievement of wide conversion ratio, minimization of voltage stresses across the semiconductors, and high efficiency, while also reducing component count as much as possible.

Distinct strategies can be used in order to achieve high voltage step-up without using transformers. For instance, coupled inductors are adequate for this purpose, although the existing leakage inductance typically affects the converter efficiency significantly and also the voltage stresses across the main switches (Himmelstoss and Wurm, 2000). Cascaded converters are also able to extend the static gain of classical dc-dc converters, being a single and straightforward approach. However, the overall efficiency is drastically affected if many conversion stages are adopted, with consequent increase of component count (Novaes, Rufer and Barbi, 2007). Recent topologies also include the use of voltage multiplier cells (VMCs) associated to interleaved boost converters, which are adequate for high-current, high-power applications with wide conversion ratio at the cost of increased number of semiconductors.

Considering the availability of distinct solutions available in literature, sometimes it is hard to choose a proper topology for a specific application and operating point. Within this context, this work proposes a comparative analysis among three types of nonisolated boost-type dc-dc converters, that are the classical boost converter, the quadratic boost converter, and the boost converter based on the three-state switching cell using voltage multipliers cells (3SSC-VMC). The commutated power concept is used for this purpose, as it is possible to properly compare them from the point of view of stresses regarding the semiconductor elements. Firstly, some basic concepts are reviewed and a theoretical analysis is carried out. The obtained results are then supposed to demonstrate that it is possible to choose a proper solution without the need to carry out an extensive and complex analysis that would typically involve the implementation of several converter prototypes, which may not be feasible in practice.

2. Review of The Commutated Power Concept

The stresses involving semiconductors certainly play an important role in the practical selection of a proper converter topology for a particular application, thus affecting overall cost, efficiency, and dimensions of the resulting structure (Kolar and Ertl, 1999). The evaluation of the loss mechanism is only a trivial task in converters with a reduced number of components e.g. the classical dc-dc converters (Figueiredo, Tofoli and Alves, 2011), (Lemos et. al, 2015). However, significant effort is necessary in order to estimate the losses in more complex topologies. Hence, it is interesting to establish simple and straightforward criteria in order to perform a proper comparative analysis regarding voltage and current stresses in semiconductors.

Considering the performance evaluation of power converters from the efficiency point of view, literature presents numerous related examples, which are typically focused on quantitative approaches involving complex and detailed analyses (Cavalcanti et al, 2003). The commutated power concept was introduced by (Figueiredo, Tofoli and Alves, 2011), which corresponds to the total amount of power processed by a given semiconductor and must not be misled with the switching losses. Moreover, a proper comparison among the classical nonisolated dc-dc converters i.e. buck, boost, buck-boost, Ćuk, SEPIC (single-ended primary inductance converter) and zeta

was also presented. It can be stated that the higher the commutated power is, the higher the semiconductor losses are, which have direct impact on efficiency are directly related to the existing voltage and current stresses.

In order to determine the commutated power in a semiconductor element, it is assumed that both filter inductor and filter capacitor are large enough so that the high-frequency ripples are neglected. The power commutated by a generic semiconductor element is the product between the maximum blocking voltage V_{max} and the maximum current flowing through it I_{max} i.e.:

$$P_C = V_{\max} \cdot I_{\max} \tag{1}$$

This is a qualitative concept that has been also applied to the classical isolated dc-dc converters in (Lemos et. al, 2015) i.e. one switch-forward, two switch-forward, *push-pull*, half-bridge, and full-bridge converters. The analysis is also strictly focused on the voltage and current stresses regarding switches and diodes analogously to the study carried out by (Figueiredo, Tofoli and Alves, 2011).

The expressions for the total commutated power normalized as a function of the output power in the classical dc-dc converter topologies operating in continuous conduction mode (CCM) are summarized in Table I. It is then possible to compare them using a simple concept that can be extended to any type of power converter independently on the circuit complexity. For instance, let us consider that the buck-boost, Ćuk, SEPIC and zeta converters are designed for the same operating conditions. Since the commutated power depends only on the duty cycle, it can be seen that all topologies are supposed to present the very same losses regarding the semiconductors. However, the overall efficiency depends on other key issues e.g. parasitic elements such as the intrinsic series resistances of inductors and capacitors.

It has been effectively demonstrated by (Tofoli et al, 2012) that the very static gain is reduced in practice due to the presence of the inductor series resistance R_L in the dc-dc boost converter. Efficiency also drops drastically as R_L increases, what becomes more evident at high power levels. This is due to the increase of losses in R_L with the square of the rms current through the inductor. Other issues related to the equivalent series resistance of the output capacitor, reverse recovery losses, and high *dv*/*dt* and *di*/*dt* rates associated with the rectifier diode will cause a significant reduction of overall efficiency. Therefore, the conventional boost converter does not become an adequate choice for applications that demand wide conversion ratio. In this case, other solutions can be considered e.g. the quadratic boost converter and the 3SSC-VMC boost converter, which will be analyzed as follows from the point of view of the commutated power.

3. Analysis of The Commutated Power in Boost-Based Dc-Dc Converters

3.1 Conventional Boost Converter

As it was mentioned before, the dc-dc boost converter shown in Figure 1 is a popular choice in voltage step-up applications. However, the conversion ratio is limited due to appreciable losses in the filter inductor that exist when high values of the duty cycle are necessary. It is then expected that the power "commutated" by the filter inductor brings significant information on the losses associated to the filter inductor, as the study developed by (Figueiredo, Tofoli and Alves, 2011) and (Lemos et. al, 2015) can be used for this purpose.

Analyzing the operating stages in the ideal boost converter while neglecting the high-frequency ripples, it can be seen that the maximum current $I_{L(\max)}$ and the absolute value of the maximum voltage $V_{L(\max)}$ are:

$$V_{L(\max)} = V_o - (1-D)\cdot V_o \tag{2}$$

$$I_{L(\max)} = \frac{I_o}{(1-D)} \tag{3}$$

Table I. Total commutated power normalized as a function of the output power in the classical dc-dc converters

Topology	Total Commutated Power
Buck converter	$\overline{P_{C(\text{total})(SD)}} = \frac{2}{D}$
Boost converter	$\overline{P_{C(\text{total})(SD)}} = \frac{2}{1-D}$
Buck–boost, Ćuk, SEPIC, and zeta converters	$\overline{P_{C(\text{total})(SD)}} = \frac{2}{D\cdot(1-D)}$
One-switch and two-switch-forward converters	$\overline{P_{C(\text{total})(SD)}} = \frac{4.88}{D}$
Push-pull converter	$\overline{P_{C(\text{total})(SD)}} = \frac{8}{D}$
Half-bridge and full-bridge converters	$\overline{P_{C(\text{total})(SD)}} = \frac{8.8}{D}$

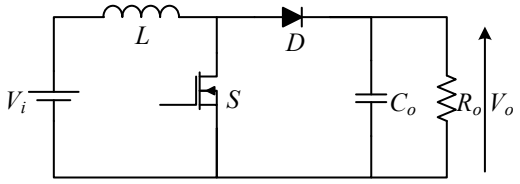


Figure 1. Dc-dc boost converter.

where V_o is the output voltage, I_o is the output current, and D is the duty cycle.

Besides, the "commutated" power in the inductor is given by:

$$P_{C(L)} = V_{L(\max)} \cdot \mathrm{I}_{L(\max)} \tag{4}$$

Substituting (2) and (3) in (4), gives:

$$P_{C(L)} = \frac{D\cdot P_o}{(1-D)} \tag{5}$$

where P_o is the output power.

It is also possible to normalize (5) as a function of the output power:

$$\overline{P_{C(L)}} = \frac{D}{(1-D)} \tag{6}$$

Finally, considering the expression for the commutated power in the semiconductor elements according to Table I, the total commutated power in the boost converter is represented by:

$$\overline{P_{\text{C(total)(boost)}}} = \overline{P_{\text{C(total)}(SD)}} + \overline{P_{C(L)}} = \frac{2+D}{(1-D)} \tag{7}$$

3.2 Quadratic Boost Converter

Quadratic converters allow obtaining high voltage step-up or step-down by simply considering that the total static gain is equal to the product between the static gains of two individual converters. This concept allows extending the static gain by cascading as many converters as necessary. However, efficiency is significantly reduced and high component count is a significant drawback. The static gain of the single-switch quadratic boost converter presented in Figure 2 is given by:

$$G = \frac{V_o}{V_i} = \frac{1}{(1-D)^2} \tag{8}$$

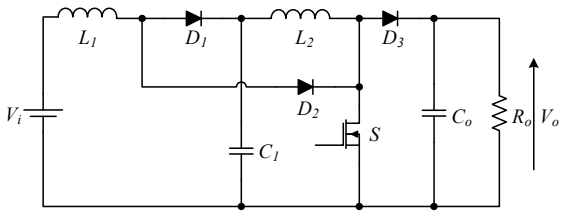


Figure 2. Dc-dc quadratic boost converter.

If the output voltage is very high, the voltage stresses across the main switch S and diode D_3 are appreciable i.e. equal to the output voltage, thus leading to the use of costly components and poor efficiency. The reverse recovery problem in such diode and also stability are also of major concern. Besides, increased complexity in terms of the control system is expected because the converter behaves as a fourth-order system.

The analysis performed by (Figueiredo, Tofoli and Alves, 2011) and (Lemos et. al, 2015) can also be applied to the topology in Figure 2. The detailed analysis of the converter will not be presented in this work, but it can be easily demonstrated that the current and voltage stresses can be determined from expressions

$$I_{S(\text{avg})} = \frac{D \cdot I_o \cdot (2-D)}{(1-D)^2} \tag{9}$$

$$I_{S(rms)} = \frac{I_o \cdot (2-D) \cdot \sqrt{D}}{(1-D)^2} \tag{10}$$

$$V_{S(\max)} = V_o \tag{11}$$

$$I_{D1(\text{avg})} = \frac{D \cdot I_o}{(1-D)^2} \tag{12}$$

$$I_{D1(rms)} = \frac{I_o \cdot \sqrt{D}}{(1-D)^2} \tag{13}$$

$$V_{D1(\max)} = \frac{D \cdot \mathrm{V}_i}{(1-D)^2} \tag{14}$$

$$I_{D2(\text{avg})} = \frac{I_o}{1-D} \tag{15}$$

$$I_{D2(rms)} = \frac{I_o \cdot \sqrt{1-D}}{(1-D)} \tag{16}$$

$$V_{D2(\max)} = V_o \cdot (1-D) \tag{17}$$

$$I_{D3(\text{avg})} = I_o \tag{18}$$

$$I_{D3(rms)} = \frac{I_o \cdot \sqrt{1-D}}{(1-D)} \tag{19}$$

$$V_{D3(\max)} = V_o \tag{20}$$

After some mathematical manipulations, it can be demonstrated that the total commutated power in the semiconductor devices (SD) normalized as a function of the output power is given by:

$$\overline{P_{\text{C(total)(SD)}}} = \frac{2 \cdot (2-D)}{(1-D)^2} \tag{21}$$

If the same procedure developed in the previous section for the conventional boost converter is applied to inductors L_1 and L_2, the commutated power in such elements is then given by:

$$\overline{P_{\text{C}(L1)}} = \frac{D}{(1-D)} \tag{22}$$

$$\overline{P_{\text{C}(L2)}} = \frac{D}{(1-D)} \tag{23}$$

The total commutated power considering both semiconductors and magnetics is:

$$\begin{aligned} \overline{P_{C(\text{total})(quad)}} &= \overline{P_{\text{C(total)(S}D)}} + \overline{P_{\text{C}(L1)}} + \overline{P_{\text{C}(L2)}} \\ &= \frac{2 \cdot (2-\mathrm{D}^2)}{(1-D)^2} \end{aligned} \tag{24}$$

3.3 3SSC-VMC Boost Converter

The 3SSC-VMC boost converter was proposed in (Tofoli et al, 2012) as an interesting solution for high-current, high-power applications with high voltage step-up applications. This is a modular approach that allows extending the static gain as more VMCs are added, at the cost of high component count. However, the advantages addressed to the 3SSC are maintained e.g. reduction of size, weight, and volume of magnetics, which are designed for twice the switching frequency. A generic version of the topology with several VMCs is represented in Figure 3, while its respective static gain is:

$$G_v = \frac{V_o}{V_i} = \frac{VMC+1}{1-D} \tag{25}$$

where VMC corresponds to number of multiplier stages.

It can be seen that the conversion ratio in this case does not depend only on the duty cycle, but also on the number of VMCs. Then it is not necessary to

use extreme values of duty cycle in order to achieve wide conversion ratios, leading to the significant reduction of copper losses in the filter inductor.

The theoretical analysis for the calculation of current and voltage stresses in the semiconductor elements was performed in (Tofoli et al, 2012). Expressions (26) to (31) can be used to design the active switches and diodes that constitute the 3SSC.

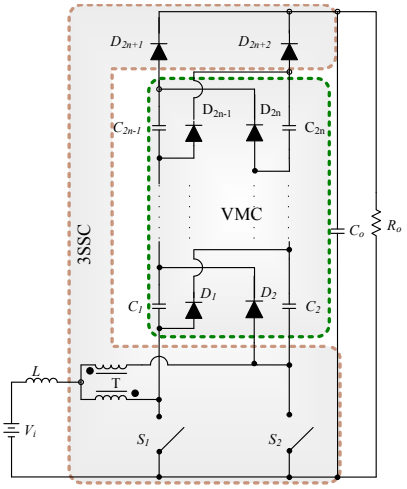


Figure 3. Dc-dc 3SSC-VMC boost converter.

$$I_{S(avg)} = \frac{I_i \cdot (\mathrm{D}+VMC)}{2 \cdot (VMC+1)} \tag{26}$$

$$I_{S(rms)} = \frac{I_i \cdot \sqrt{(D+VMC)}}{2 \cdot (VMC+1)} \tag{27}$$

$$V_{S(\max)} = \frac{\left(\frac{V_o}{2} + \frac{\Delta V_c}{8}\right)}{VMC^{0.3}} \tag{28}$$

$$I_{D(avg)} = \frac{I_i \cdot (1-D)}{2 \cdot (VMC+1)} \tag{29}$$

$$I_{D(rms)} = \frac{I_i \cdot \sqrt{(1-D)}}{2 \cdot (VMC+1)} \tag{30}$$

$$V_{D(\max)} = \frac{\left(\frac{V_o}{2} + \frac{\Delta V_c}{8}\right)}{VMC^{0.3}} \tag{31}$$

where I_i is the average input current.

On the other hand, expressions (32) to (34) are valid for the diodes that constitute the VMC.

$$I_{DM(avg)} = \frac{I_i \cdot (1-D)}{2 \cdot (VMC+1)} \tag{32}$$

$$I_{DM(rms)} = \frac{I_i \cdot \sqrt{(1-D)}}{2 \cdot (VMC+1)} \tag{33}$$

$$V_{DM(\max)} = 2 \cdot \frac{\left(\frac{V_o}{2} + \frac{\Delta V_c}{8}\right)}{VMC^{0.3}} \tag{34}$$

If the commutated power concept is applied to the semiconductors in the 3SSC-VMC boost converter, expression (35) is then obtained.

$$\overline{P_{C(\text{total})(\text{SD})}} = \frac{(VMC+1) \cdot (VMC+2)}{2 \cdot VMC^{0.3} \cdot (1-D)} \tag{35}$$

The same procedure can be carried out for the filter inductor and gives:

$$\overline{P_{C(\text{L})}} = \frac{0.15 \cdot (VMC+1)}{(1-D)} \tag{36}$$

The total commutated power considering both semiconductors and magnetics (except for the autotransformer of the 3SSC) is:

$$\overline{P_{C(\text{total})(3\text{SSC}-\text{VMC})}} = \frac{VMC+1}{1-D} \cdot \left(\frac{(VMC+2)+0.3 \cdot VMC^{0.3}}{2 \cdot VMC^{0.3}} \right) \tag{37}$$

4. Validation of The Commutated Power Curves And Discussion of Results

As it was mentioned before, the classical dc-dc boost converter is not adequate for high voltage step-up due to the significant losses that exist in the filter inductor in practical applications. In order to establish a fair comparison and evaluate losses properly using the proposed concept of the commutated power, the quadratic boost converter and the 3SSC-VMC boost converter were designed according to the specifications and operating point given in Table II.

Firstly, it can be seen that the inductors used in the converters shown in Figure 1 and Figure 2 present appreciable dimensions, mainly because the input current is high. Besides, they operate at the switching frequency, unlike the magnetic elements used in the 3SSC-based converter.

The expressions for the commutated power in the nonisolated boost-based dc-dc converters were developed in Section 3. It is quite interesting to validate the theoretical curves that can be plotted as a function of the duty cycle from expressions (7), (24), and (37). For this purpose, software PSIM® is employed, where the parameters given in Table II are maintained constant, except for the duty cycle, which is varied from 0.1 to 0.9 considering steps of 0.1. The comparison between the curves is presented in Figure 4.

According to Figure 4 (a), it can be seen that the commutated power in the conventional boost converter is low especially at reduced values of the duty cycle i.e. if wide conversion ratio is not necessary. In this case, it is supposed to present improved efficiency in terms of reduced losses in the semiconductor elements and the filter inductor. However, if the operating point defined in Table II is considered, the output voltage is more than eight times higher than the input voltage and the conventional boost converter does not become a viable choice as it will be demonstrated by the results discussed as follows.

Since the quadratic boost converter presents two inductors and higher component count, the curve in Figure 4 (b) shows that the commutated power is high even at low values of the duty cycle, although it is possible to achieve wide conversion ratios without the need of extreme values of the duty cycle in this case.

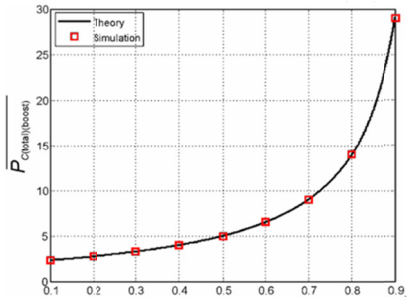
The 3SSC-VMC boost converters represented by the curves in Figure 4 (c) to (e) are adequate for high voltage step-up, while tradeoffs can be made between the duty cycle and component count, being this an adequate approach for high-current applications. Of course, the commutated power increases as the number of VMCs also does. Consequently, efficiency tends to be reduced due to the increase in the number of diodes in the additional VMCs.

In order to establish a proper comparison among the aforementioned converters, the commutated power for each one of them has been determined according to the theoretical study carried out in Section 3 and their respective expressions, while the results are presented in Table III. Considering the classical boost converter (topology A), it can be seen that the commutated power in the inductor is the highest one among all topologies. In other terms, the copper losses in this case are supposed to be significant due to the high current flowing through the inductor, leading to reduced efficiency. Additionally, the total commutated power in topology A is less than that in the quadratic boost converter (topology B) since the latter topology presents higher component count, whose stresses are also significant. Finally, it is easy to notice that the total commutated power increases as the number of VMCs also does in topologies C, D, and E.

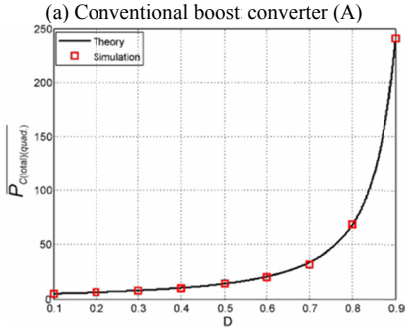
The quadratic boost converter is supposed to present the worst efficiency for the operating point defined in Table II according to the results in Table III. In order to validate this assumption, the overall losses considering all semiconductor elements and inductors have been calculated for the rated condition. It is worth to mention that conduction and switching losses have been considered in all semiconductor elements. In addition, the core and copper losses have been estimated in the inductors. According to Table IV, the best efficiency is achieved by the 3SSC-based boost converter where *VMC*=1 (E). On the other hand, the quadratic boost converter presents the worst performance.

5. Conclusion

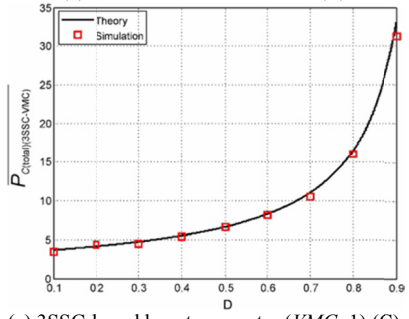
According to the developed study, it can be seen that the commutated power concept can be employed for qualitative comparison purposes, since it is based on the very characteristics of the power converter topology. If high voltage step-up is necessary, the 3SSC-VMC boost converters are supposed to present improved performance in terms of increased efficiency if compared with the remaining topologies analyzed in this work.



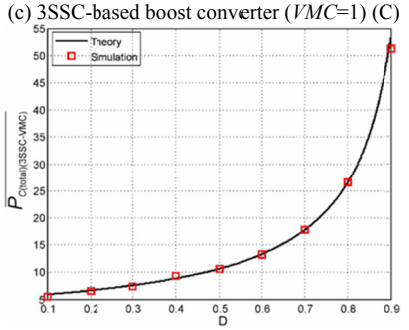
(a) Conventional boost converter (A)



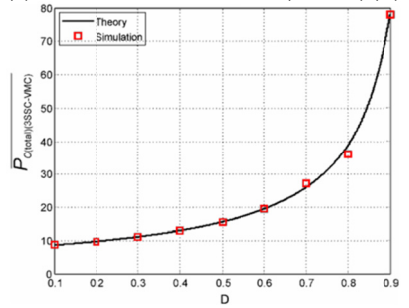
(b) Quadratic boost converter (B)



(c) 3SSC-based boost converter (*VMC*=1) (C)



(d) 3SSC-based boost converter (*VMC*=2) (D)



(e) 3SSC-based boost converter (*VMC*=3) (E)

Figure 4. Comparison between the theoretical curves of the commutated power and simulation results.

Table II. Specifications of boost-based dc-dc converters.

Parameter	Design Specifications of The Boost-Type Topologies				
	(A)	(B)	(C)	(D)	€
Dc input voltage	V_i=48 V	V_i=48 V	V_i=48 V	V_i=48 V	V_i=48 V
Dc output voltage	V_o=400 V	V_o=400 V	V_o=400 V	V_o=400 V	V_o=400 V
Rated duty cycle	D=0.88	D=0.654	D=0.790	D=0.685	D=0.580

Rated output power	P_o=1000 W	P_o=1000 W	P_o=1000 W	P_o=1000 W	P_o=1000 W
Switching frequency	f_s=25 kHz	f_s=25 kHz	f_s=25 kHz	f_s=25 kHz	f_s=25 kHz
Ripple current through the inductor(s)	$\Delta I_L = 0.15 \cdot I_i$	$\Delta I_L = 0.15 \cdot I_i$	$\Delta I_L = 0.15 \cdot I_i$	$\Delta I_L = 0.15 \cdot I_i$	$\Delta I_L = 0.15 \cdot I_i$
Ripple voltage across the capacitor(s)	$\Delta V_o = 0.05 \cdot V_o$	$\Delta V_o = 0.05 \cdot V_o$	$\Delta V_o = 0.05 \cdot V_o$	$\Delta V_o = 0.05 \cdot V_o$	$\Delta V_o = 0.05 \cdot V_o$
Inductor(s)	L_b=4.5 mH, core NEE 100/59/27, 257 turns, 2×AWG 19	L_1=3.34 mH, core NEE 100/59/27, 190 turns, 2×AWG 19 L_2=9.66 mH, core NEE 100/59/27, 127 turns, 1×AWG 19	L=130 μH, toroidal core 58195A2, 22 turns,1×AWG 26	L=70 μH, toroidal core 58195A2, 22 turns, 1×AWG 26	L=70 μH, toroidal core 58195A2. 22 turns, 1×AWG 26
Autotransformer	–	–	NEE 55/28/21, N_p=28 turns, N_s=28 turns, 2×AWG 26	NEE 55/28/21, N_p=28 turns, N_s=28 turns, 2×AWG 26	NEE 55/28/21, N_p=28 turns, N_s=28 turns, 2×AWG 26
Capacitor(s)	C_o=4.4 μF	C_1=9.434 μF C_o=3.2 μF	C_1=C_2=2.2 μF C_o=670 μF	C_1=C_2=4.4 μF C_3=C_4=2.2 μF C_o=670 μF	C_1=C_2=4.4 μF C_3=C_4=3.2 μF C_5=C_6=2.2 μF C_o=670 μF
Main switch(es)	MOSFET 2SK3131	MOSFET 2SK3131	MOSFET IRFP4247	MOSFET IRFP4247	MOSFET IRFP4247
Diode(s)	Ultrafast diode HFA25PB60	Ultrafast diode HFA25PB60	Ultrafast diode HFA25PB60	Ultrafast diode HFA25PB60	Ultrafast diode HFA25PB60

Table III. Calculation of the commutated power in the dc-dc converters.

Topology	Commutated Power in The Semiconductors	Commutated Power in The Inductor(s)	Total Commutated Power
A	16.667	7.333	24.000
B	22.489	3.780	26.269
C	14.286	1.428	15.714
D	15.460	1.428	16.888
E	17.119	1.428	18.547

Table IV. Calculation of losses in the dc-dc converters

Topology	Inductor Losses [W]	Diode Losses [W]	Switch Losses [W]	Theoretical Efficiency (%)
A	248.04	6.97	94.73	74.09
B	200.05	48.55	109.14	73.63
C	12.28	11.88	12.18	96.46
D	12.63	18.14	12.92	95.82
E	12.17	19.88	12.24	95.75

Since the intrinsic series resistance of the filter inductor plays an important role in the overall efficiency, it is expected that the analysis of the power "commutated" by such magnetic element brings important information on the existing losses, since copper losses increase with the square of the rms current through. If the commutated power in the inductor is neglected in low conversion ratios, the qualitative analysis is not supposed to present significant errors. However, at high values of the duty cycle, the involved losses become appreciable, thus contributing to the sensitive minimization of efficiency.

The proposed approach can be seen as a simple and decisive criterion for the simultaneous comparison among several power converters considering their performance in terms of existing losses in semiconductors and magnetic elements. It has then been demonstrated that losses increase as the total commutated power also does.

Acknowledgement

The authors acknowledge CAPES, CNPq, FAPEMIG, and INERGE for the support to this work.

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